IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 2, 4-8, 11-20, 22-26 and 29-36 and CANCEL claims 37-48 in accordance with the following. Claims 3, 9, 10, 21, 27, 28 are designated withdrawn.

1. (CURRENTLY AMENDED) A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

~~a first detection step for~~ detecting, before said board is covered with a first insulating layer, the actual position of a first electronic component formed on a surface of said board;

~~a first holding step for~~ calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component on the surface of said board, and ~~for~~ holding said displacement as first displacement data; and

~~a first correction step for~~ correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer.

2. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 1, further comprising ~~a first maskless exposure step for~~ applying, based on said design data corrected in said ~~first correction step~~correcting, a maskless exposure to said board covered with said first insulating layer.

3. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 1, further comprising a first direct patterning step for forming, based on said design data corrected in said first correction step, a wiring pattern by inkjetting on said board covered with said first insulating layer.

4. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 1, further comprising ~~a first via formation step for~~ forming, based on said design data corrected in said ~~first correction step~~correcting, a via hole in said board covered with said first insulating layer.

5. (CURRENTLY AMENDED) A component-embedded board fabrication method as

claimed in claim 1, further comprising:

~~a second detection step for~~ detecting, before said board is covered with a second insulating layer, the actual position of a second electronic component formed on a surface of said first insulating layer in which said first electronic component is already embedded;

~~a second holding step for~~ calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component on the surface of said first insulating layer, and ~~for~~ holding said displacement as second displacement data; and

~~a second correction step for~~ correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

6. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 1, further comprising:

~~a first imaging step for~~ capturing, before said board is covered with a second insulating layer, an image of a surface of said first insulating layer on which a second electronic component is formed and in which said first electronic component is already embedded;

~~a second holding step for~~ calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component detected from second image data obtained by imaging the surface of said first insulating layer, and ~~for~~ holding said displacement as second displacement data; and

~~a second correction step for~~ correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

7. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 5, further comprising ~~a second maskless exposure step for~~ applying, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a maskless exposure to said board covered with said second insulating layer.

8. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 6, further comprising ~~a second maskless exposure step for~~ applying, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a maskless exposure to said board covered with said second insulating layer.

9. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 5, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board

covered with said second insulating layer.

10. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 6, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board covered with said second insulating layer.

11. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 5, further comprising ~~a second via formation step for~~ forming, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a via hole in said board covered with said second insulating layer.

12. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 6, further comprising ~~a second via formation step for~~ forming, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a via hole in said board covered with said second insulating layer.

13. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 1, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said ~~first correction step~~correcting corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

14. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 1, wherein when the actual position of a terminal of said formed electronic component is displaced from the position specified by said design data and intersects with a wiring line used for connection to a terminal of another electronic component, said ~~first correction step~~correcting corrects said design data so as to move said wiring line away from the terminal of said other electronic component.

15. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 5, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

16. (CURRENTLY AMENDED) A component-embedded board fabrication method as

claimed in claim 5, wherein when the actual position of a terminal of said formed electronic component is displaced from the position specified by said design data and intersects with a wiring line used for connection to a terminal of another electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said wiring line away from the terminal of said other electronic component.

17. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 6, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

18. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 6, wherein when the actual position of a terminal of said formed electronic component is displaced from the position specified by said design data and intersects with a wiring line used for connection to a terminal of another electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said wiring line away from the terminal of said other electronic component.

19. (CURRENTLY AMENDED) A component-embedded board fabrication method for fabricating a component-embedded board with electronic components embedded within a wiring board, comprising:

~~a first imaging step for~~ capturing, before said board is covered with a first insulating layer, an image of a surface of said board on which a first electronic component is formed;

~~a first holding step for~~ calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component detected from first image data obtained by imaging the surface of said board, and ~~for~~ holding said displacement as first displacement data; and

~~a first correction step for~~ correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer.

20. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 19, further comprising ~~a first maskless exposure step for~~ applying, based on said design data corrected in said ~~first correction step~~correcting, a maskless exposure to said

board covered with said first insulating layer.

21. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 19, further comprising a first direct patterning step for forming, based on said design data corrected in said first correction step, a wiring pattern by inkjetting on said board covered with said first insulating layer.

22. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 19, further comprising ~~a first via formation step for~~ forming, based on said design data corrected in said ~~first correction~~correcting ~~step~~, a via hole in said board covered with said first insulating layer.

23. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 19, further comprising:

~~a first detection step for~~ detecting, before said board is covered with a second insulating layer, the actual position of a second electronic component formed on a surface of said first insulating layer in which said first electronic component is already embedded;

~~a second holding step for~~ calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component on the surface of said first insulating layer, and ~~for~~ holding said displacement as second displacement data; and

~~a second correction step for~~ correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

24. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 19, further comprising:

~~a second imaging step for~~ capturing, before said board is covered with a second insulating layer, an image of a surface of said first insulating layer on which a second electronic component is formed and in which said first electronic component is already embedded;

~~a second holding step for~~ calculating a displacement between the design position of said second electronic component and the actual position of said second electronic component detected from second image data obtained by imaging the surface of said first insulating layer, and ~~for~~ holding said displacement as second displacement data; and

~~a second correction step for~~ correcting, based on said second displacement data, design data to be used for processing said board after said board is covered with said second insulating layer.

25. (CURRENTLY AMENDED) A component-embedded board fabrication method as

claimed in claim 23, further comprising ~~a second maskless exposure step for~~ applying, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a maskless exposure to said board covered with said second insulating layer.

26. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 24, further comprising ~~a second maskless exposure step for~~ applying, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a maskless exposure to said board covered with said second insulating layer.

27. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 23, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board covered with said second insulating layer.

28. (WITHDRAWN) A component-embedded board fabrication method as claimed in claim 24, further comprising a second direct patterning step for forming, based on said design data corrected in said second correction step, a wiring pattern by inkjetting on said board covered with said second insulating layer.

29. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 23, further comprising ~~a second via formation step for~~ forming, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a via hole in said board covered with said second insulating layer.

30. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 24, further comprising ~~a second via formation step for~~ forming, based on said design data corrected in said correcting, based on said second displacement data~~second correction step~~, a via hole in said board covered with said second insulating layer.

31. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 19, wherein when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said ~~first correction step~~correcting corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

32. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 19, wherein when the actual position of a terminal of said formed electronic component is displaced from the position specified by said design data and intersects with a wiring line used for connection to a terminal of another electronic component, said ~~first~~

~~correction step~~correcting corrects said design data so as to move said wiring line away from the terminal of said other electronic component.

33. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 23 wherein, when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

34. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 23 wherein, when the actual position of a terminal of said formed electronic component is displaced from the position specified by said design data and intersects with a wiring line used for connection to a terminal of another electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said wiring line away from the terminal of said other electronic component.

35. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 24 wherein, when the actual position of a terminal of said formed electronic component is displaced from an end of a wiring line that is defined in said design data as being the end to be connected to the terminal of said electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said end of said wiring line to be connected to the terminal of said electronic component to the actual position of said formed electronic component.

36. (CURRENTLY AMENDED) A component-embedded board fabrication method as claimed in claim 24 wherein, when the actual position of a terminal of said formed electronic component is displaced from the position specified by said design data and intersects with a wiring line used for connection to a terminal of another electronic component, said correcting, based on said second displacement data, ~~second correction step~~ corrects said design data so as to move said wiring line away from the terminal of said other electronic component.

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